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JC891 U.S. PTO
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UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
PNET.011D

Total Pages in this Submission
3

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

SEMICONDUCTOR DEVICE, SEMICONDUCTOR PACKAGE FOR USE THEREIN, AND MANUFACTURING METHOD THEREOF

JC927 U.S. PTO
09/689824
10/13/00

and invented by:

SASAKI, Takaaki

If a CONTINUATION APPLICATION, *check appropriate box and supply the requisite information:*

☐ **Continuation** ☒ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: **09/062,720**

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having **30** pages and including the following:
   - a. ☒ Descriptive Title of the Invention
   - b. ☐ Cross References to Related Applications *(if applicable)*
   - c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*
   - d. ☐ Reference to Microfiche Appendix *(if applicable)*
   - e. ☒ Background of the Invention
   - f. ☒ Brief Summary of the Invention
   - g. ☒ Brief Description of the Drawings *(if drawings filed)*
   - h. ☒ Detailed Description
   - i. ☒ Claim(s) as Classified Below
   - j. ☒ Abstract of the Disclosure

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Docket No. PNET.011D
Total Pages in this Submission 3

Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
   a. ☒ Formal Number of Sheets 6
   b. ☐ Informal Number of Sheets _____
4. ☒ Oath or Declaration
   a. ☐ Newly executed *(original or copy)* ☐ Unexecuted
   b. ☒ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*
   c. ☐ With Power of Attorney ☐ Without Power of Attorney
   d. ☐ *DELETION OF INVENTOR(S)*
   Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).
5. ☒ Incorporation By Reference *(usable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Computer Program in Microfiche *(Appendix)*
7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*
   a. ☐ Paper Copy
   b. ☐ Computer Readable Copy *(identical to computer copy)*
   c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☐ Assignment Papers *(cover sheet & document(s))*
9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*
10. ☐ English Translation Document *(if applicable)*
11. ☒ Information Disclosure Statement/PTO-1449 ☐ Copies of IDS Citations
12. ☒ Preliminary Amendment
13. ☒ Acknowledgment postcard
14. ☐ Certificate of Mailing
    ☐ First Class ☐ Express Mail *(Specify Label No.):* _____

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Total Pages in this Submission 3

Accompanying Application Parts (Continued)

15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☐ Additional Enclosures *(please identify below):*

Request That Application Not Be Published Pursuant To 35 U.S.C. 122(b)(2)

17. ☐ Pursuant to 35 U.S.C. 122(b)(2), Applicant hereby requests that this patent application not be published pursuant to 35 U.S.C. 122(b)(1). Applicant hereby certifies that the invention disclosed in this application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication of applications 18 months after filing of the application.

Warning

An applicant who makes a request not to publish, but who subsequently files in a foreign country or under a multilateral international agreement specified in 35 U.S.C. 122(b)(2)(B)(i), must notify the Director of such filing not later than 45 days after the date of the filing of such foreign or international application. A failure of the applicant to provide such notice within the prescribed period shall result in the application being regarded as abandoned, unless it is shown to the satisfaction of the Director that the delay in submitting the notice was unintentional.

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Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra		Rate	Fee
Total Claims	17	- 20 =	0	x	$18.00	$0.00
Indep. Claims	3	- 3 =	0	x	$80.00	$0.00
Multiple Dependent Claims (check if applicable) ☐						$0.00
					BASIC FEE	$710.00
OTHER FEE ***(specify purpose)***						$0.00
					TOTAL FILING FEE	$710.00

☒ A check in the amount of **$710.00** to cover the filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. **50-0238** as described below. A duplicate copy of this sheet is enclosed.

- ☐ Charge the amount of as filing fee.
- ☒ Credit any overpayment.
- ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).

Signature

Dated: **OCT. 13, 2000**

ADAM C. VOLENTINE
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cc:

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION of

Takaaki SASAKI [Group Art Unit: 2822]

New Divisional of Serial No. 09/062,720 [Examiner: T. M. Arroyo]

Filed: October 13, 2000

For: SEMICONDUCTOR DEVICE, SEMICONDUCTOR PACKAGE FOR USE THEREIN, AND MANUFACTURING METHOD THEREOF

PRELIMINARY AMENDMENT

Honorable Assistant Commission of Patents and Trademarks,
Washington, D.C. 20231

Sir:

Preliminary to the examination of the above-identified application, please enter the following amendments and consider the following remarks:

In the Abstract

Kindly amend the Abstract of the Disclosure as follows:

Line 2, change "comprised of" to -- includes -- .

Line 3, change "element" to -- chip -- .

Line 4, change "through" to -- elongate opening -- .

Line 5, delete "hall"; and change "element" to -- chip -- .

Line 6, delete "where the element is formed".

Line 7, after "being" insert -- aligned -- ; and change "through hall" to -- elongate opening -- .

Line 8, change "element" to -- chip -- .

Line 9, change "through" to -- elongate opening -- .

Line 10, delete "hall"; and change "through hall" to -- elongate opening -- .

In the Specification

Kindly amend the specification as follows:

Page 1, between lines 3 and 4, insert

--CROSS REFERENCE TO RELATED APPLICATIONS

This is a divisional application of application Serial No. 09/062,720, filed April 20, 1998, which is hereby incorporated by reference in its entirety for all purposes.--

Page 1, lines 7 and 18, change "device" to -- chip -- .

Page 1, line 7, change "of" (second occurrence) to -- as -- .

Page 1, line 18, change "side of" to -- size as -- .

Page 2, lines 1, 2, 13, and 16, change "element" to -- chip -- .

Page 3, lines 3, 6, 9, 14, and 19, change "element" to -- chip -- .

Page 4, lines 7, 11, 17, 20 and 22, change "element" to -- chip -- .

Page 5, lines 2, 6, 11, 15 and 16, change "element" to -- chip -- .

Page 6, line 1, change "of" (second occurrence) to -- as -- .

Page 6, line 2, change "meeting" to -- meets -- .

Page 6, lines 2, 10 (first occurrence), 11, 13, 19 (second occurrence) and 21, change "element" to -- chip -- .

Page 6, lines 14, 16 and 22, change "through hall" to -- elongate opening -- .

Page 7, lines 2, 7, 13, 14, 18 and 19, change "element" to -- chip -- .

Page 7, lines 16, 20 and 22 (both occurrences), change "through hall" to -- elongate opening -- .

Page 8, lines 5, 8, 10, 11, 14, 21 and 22, change "element" to -- chip -- .

Page 8, line 6, change "through hall" to -- elongate opening -- .

Page 9, lines 4, 6, 8, 13 (second occurrence), 16, 18, 19 and 22, change "element" to -- chip -- .

Page 9, lines 2, 6, 8, 9 and 15, change "through hall" to -- elongate opening -- .

Page 10, line 15, change "element" to -- chip -- .

Page 11, line 17, change "element" to -- chip -- .

Page 12, lines 2, 3 (second occurrence) and 10, change "element" to -- chip -- .

Page 12, lines 7, 8, 13-14 and 21, change "through hall" to -- elongate opening -- .

Page 13, lines 11, 13 and 19, change "element" to -- chip -- .

Page 13, lines 1, 2, 6, 17, 19 and 21, change "through hall" to -- elongate opening -- .

Page 14, lines 5 and 21, change "element" to -- through hall -- .

Page 14, line 8, change "through hall" to -- elongate opening -- .

Page 15, lines 2, 4, 6, 10 and 12, change "element" to -- chip -- .

Page 15, lines 6, 15, 19 and 22, change "through hall" to -- elongate opening -- .

Page 16, lines 12, 16, 18 and 21, change "element" to -- chip -- .

Page 16, line 14, change "through hall" to -- elongate opening -- .

Page 17, line 16, change "through hall" to -- elongate opening -- .

Page 18, line 18, change "element" to -- chip -- .

Page 18, lines 16, 19 and 22, change "through hall" to -- elongate opening -- .

Page 19, lines 8 and 11, change "element" to -- chip -- .

Page 19, line 22, change "through hall" to -- elongate opening -- .

Page 20, line 2, change "through hall" to -- elongate opening -- .

Page 20, lines 18, 19 and 21, change "through halls" to -- elongate openings -- .

Page 21, line 2, change "through" to -- elongate openings -- .

Page 21, line 3, delete "halls".

Page 21, lines 3, 5, 12, 14 and 18, change "through halls" to -- elongate openings -- .

Page 21, line 9, change "element" (second occurrence) to -- chip -- .

Page 22, lines 5, 8, 11, 13, 14 and 17, change "element" to -- chip -- .

Page 23, lines 5, 6 (second occurrence), 9, 11 and 16, change "element" to

-- chip -- .

Page 23, lines 1-2 and 8, change "through hall" to -- elongate opening -- .

Page 24, lines 2, 5, 7, 9, 12 and 20 (second occurrence), change "element" to

-- chip -- .

Page 24, lines 3 and 22, change "through hall" to -- elongate opening -- .

Page 25, lines 1, 3, 5 and 8, change "element" to -- chip -- .

In the Claims

Please cancel Claims 1-6 without prejudice.

Please amend claims 10 and 11 as follows:

Claim 10, line 2, delete "8 or 9,".

Claim 11, line 2, delete "8 or 9,".

Please add new claims 12-23 as follows:

--12. A method of manufacturing a semiconductor device as claimed in claim 8, wherein the surface where the element is formed of said semiconductor element is fixed on the one side of said substrate semiconductor package via a tape-like bonding material.

13. A method of manufacturing a semiconductor device as claimed in claim 9,

wherein the surface where the element is formed of said semiconductor element is fixed on the one side of said substrate semiconductor package via a tape-like bonding material.

14. A method of manufacturing a semiconductor device as claimed in claim 8, wherein the surface where the element is formed of said semiconductor element is fixed on the one side of said substrate of said semiconductor package with adhesive.

15. A method of manufacturing a semiconductor device as claimed in claim 9, wherein the surface where the element is formed of said semiconductor element is fixed on the one side of said substrate of said semiconductor package with adhesive.

16. A semiconductor device comprising:

a substrate having a first surface and a second surface opposed to the first surface, said substrate further having an elongate opening defined therethrough from the first surface to the second surface;

a plurality of connecting patterns located on the second surface of said substrate, each of the plurality of connecting patterns having a first end;

a semiconductor chip having a surface which is mounted to the first surface of the substrate;

a plurality of electrodes located on the surface of said semiconductor chip and

aligned with said elongate opening of said substrate;

a plurality of wires extending within the elongate opening of said substrate and respectively electrically connecting said plurality of electrodes to corresponding ones of said plurality of patterns;

a resin which covers said plurality of electrodes, said plurality of wires, and the first ends of said plurality of connecting patterns; and

a solder resist which covers the side walls of the surface and the other end of said connecting patterns.

17. A semiconductor device as claimed in claim 16, wherein said substrate includes an upper plate and a lower plate which define a step configuration in the second surface of said substrate, wherein the upper plate is located between said semiconductor chip and said lower plate, and wherein the plurality of connecting patterns extend continuously from said upper plate to said lower plate such that the first end of the plurality of connecting patterns are located on said upper plate.

18. A semiconductor device comprising:

a substrate having a first surface and a second surface opposed to the first surface, said substrate further having first and second elongate openings defined therethrough from the first surface to the second surface;

a plurality of connecting patterns located on the second surface of said substrate, each of the plurality of connecting patterns having a first end;

a semiconductor chip having a surface which is mounted to the first surface of the substrate;

a plurality of electrodes located on the surface of said semiconductor chip, each of said plurality of electrodes aligned with one of said first and second elongate openings of said substrate;

a plurality of wires each extending within one of the first and second elongate openings of said substrate and respectively electrically connecting said plurality of electrodes to corresponding ones of said plurality of patterns;

a resin which covers said plurality of electrodes, said plurality of wires, and the first ends of said plurality of connecting patterns; and

a solder resist which covers the side walls of the surface and the other end of said connecting patterns.

19. A semiconductor device as claimed in claim 18, wherein said substrate includes an upper plate and a lower plate which define a step configuration in the second surface of said substrate, wherein the upper plate is located between said semiconductor chip and said lower plate, and wherein the plurality of connecting patterns extend continuously from said upper plate to said lower plate such that the first end of the

plurality of connecting patterns are located on said upper plate.

20. A semiconductor device as claimed in claim 16, wherein the elongate opening is smaller than the semiconductor chip.

21. A semiconductor device as claimed in claim 18, wherein the first and second elongate openings are smaller than the semiconductor chip.

22. A semiconductor device according to claim 16, further comprising a bonding material formed on the entire surface of the first surface of the substrate, wherein the semiconductor chip is mounted on the first surface of the substrate via the bonding material.

23. A semiconductor device according to claim 18, further comprising a bonding material formed on the entire surface of the first surface of the substrate, wherein the semiconductor chip is mounted on the first surface of the substrate via the bonding material. --

REMARKS

By this Preliminary Amendment, Claims 1-6 have been canceled, claims 10 and 11 have been revised for the purpose of eliminating multiple dependent claims, and Claims 12-23 have been added. Entry of this Preliminary Amendment is respectfully requested.

Respectfully submitted,

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Date: October 13, 2000

SEMICONDUCTOR DEVICE, SEMICONDUCTOR PACKAGE FOR USE THEREIN, AND MANUFACTURING METHOD THEREOF

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a small size semiconductor package, and more particularly, to a semiconductor package of substantially the same size of a semiconductor device referred to as a chip size package, a semiconductor device using the semiconductor device, and a manufacturing method of the semiconductor device.

2. Description of the Related Art

These days, various apparatus including semiconductor devices, particularly portable apparatus and movable apparatus are being miniaturized and lightened. Semiconductor devices for use in these apparatus are thus desired to be miniaturized and lightened accordingly.

In order to meet the demands, a package of substantially the same side of a semiconductor device referred to as a chip size package (hereinafter referred to as CSP) has recently been proposed, and some semiconductor devices using such a chip size package are implemented as products.

As a semiconductor device formed with a semiconductor

element mounted on a CSP, for example, as shown in Fig. 8, one in which a semiconductor element 3 is mounted and fixed via bumps 2 on a semiconductor package 1 is known. In this semiconductor device, the semiconductor package 1 comprises a substrate 4, a conductive connecting pattern 5 formed on one side of the substrate 4, a conductive connecting pattern 6 formed on the other side of the substrate 4, and a wiring material 7 formed so as to pierce the substrate 4 for the purpose of making the connecting pattern 5 electrically connected to the connecting pattern 6. As the material of the substrate 4, ceramics are mainly used for the purpose of making smaller the difference of the coefficient of thermal expansion between the semiconductor element 3 and the substrate 4 and thus making smaller the thermal stress to be applied to the bumps 2 and the semiconductor element 3.

The semiconductor element 3 is fixed to the substrate 4 of the semiconductor package 1 thus structured with the conductive connecting pattern 5 formed on the one side of the substrate 4 being electrically connected thereto via the bumps 2 provided on a surface 3a where the element is formed. External connecting terminals 8 such as solder balls for bonding the conductive connecting pattern 6 to a mother board (not shown) are

fixed to the conductive connecting pattern 6 formed on the other side of the substrate 4. By this, the bumps 2 of the semiconductor element 3 are electrically connected to the external connecting terminals 8 via the connecting pattern 5, the wiring material 7, and the connecting pattern 6.

The semiconductor element 3 thus mounted on the semiconductor package 1 is integrally fixed to the semiconductor package 1 by sealing the whole periphery of the junction between the substrate and the semiconductor element 3 with resin 9 referred to as underfile. It is to be noted that the resin 9 referred to as underfile also performs a function to disperse the above-mentioned thermal stress due to the difference of the coefficient of thermal expansion between the substrate 4 and the semiconductor element 3.

Fig. 9 illustrates another example of a semiconductor device formed with a semiconductor element mounted on a CSP. In Fig. 9, a semiconductor device 10 is generally referred to as a chip on board (COP). The semiconductor device 10 is formed by mounting and fixing a semiconductor element 13 via adhesive 12 or the like on a semiconductor package 11.

The semiconductor package 11 comprises a substrate 14 the material of which is glass epoxy resin or the like, a conductive

connecting pattern 15 formed on one side of the substrate 14, a conductive connecting pattern 16 formed on the other side of the substrate 14, and a wiring material 17 formed so as to pierce the substrate 14 for the purpose of making the connecting pattern 15 electrically connected to the connecting pattern 16.

A surface opposite to a surface 13a where the element is formed of the semiconductor element 13 is fixed with the adhesive 12 to one side of the substrate 14 of the semiconductor package 11 thus structured. Further, an electrode (not shown) formed on the surface 13a where the element is formed of the semiconductor element 13 is electrically connected to the connecting pattern 15 of the semiconductor package 11 via wires 18. External connecting terminals 19 such as solder balls for bonding the conductive connecting pattern 16 to a mother board (not shown) are fixed to the conductive connecting pattern 16 formed on the other side of the substrate 14. By this, the electrodes of the semiconductor element 13 are electrically connected to the external connecting terminals 19 via the connecting pattern 15, the wiring material 17, and the connecting pattern 16. The semiconductor package 11 with the semiconductor element 13 thus mounted thereon is further provided with resin 20 covering the one side of the substrate 14 and the semiconductor element 13 for

the purpose of protecting the surface 13a where the element is formed and the wires 18. By this, the semiconductor element 13 and the wires 18 are sealed with the resin 20.

However, with the semiconductor device shown in Fig. 8, in order to decrease the thermal stress between the substrate 4 and the semiconductor element 3, ceramics, which are expensive, have to be used as the material of the substrate 4, leading to high cost as a whole, which is a problem to be solved.

Further, with the semiconductor device 10 shown in Fig. 9, although, since the thermal stress between the substrate 14 and the semiconductor element 13 can be absorbed by the wires 18, glass epoxy resin, which is inexpensive, can be used as the material of the substrate 14, since the wires 18 are disposed so as to go around to the outer peripheral side of the semiconductor element 13 in this structure, the size of the semiconductor device 10 as a whole with respect to the semiconductor element 13 is large, and thus, the semiconductor device 10 can not sufficiently meet the demands for miniaturizing and thinning the semiconductor device.

SUMMARY OF THE INVENTION

The present invention is made in view of the above, and therefore an object of the invention is to provide a

semiconductor device which is of substantially the same size of a semiconductor element, which thus sufficiently meeting the demands for miniaturizing and thinning the semiconductor device, and which, at the same time, can be manufactured at a low cost, a manufacturing method thereof, and a semiconductor package suitably used in manufacturing the semiconductor device.

According to one aspect of the present invention, in order to solve the above-mentioned problem, a semiconductor package is comprised of a substrate for mounting a semiconductor element thereon to fix the side of a surface where the element is formed of the semiconductor element to one side thereof, and a connecting pattern provided on the other side of the substrate for electrical connection to the semiconductor element, the substrate being provided with a through hall formed from the one side to the other side of the substrate.

With this semiconductor package, since a through hall is formed in the substrate and the connecting pattern is provided on the side of the substrate opposite to the side on which the surface where the element is formed of the semiconductor element is mounted, an electrode formed on the surface where the element is formed of the semiconductor element and the connecting pattern can be bonded with wires through the through hall. Accordingly,

wires can be disposed without going around to the outer peripheral side of the semiconductor element. This eliminates the necessity of securing space for the wires on the outer peripheral side of the semiconductor element.

Further, since wire bonding can be carried out, the wires can absorb the difference of the coefficient of thermal expansion between the semiconductor element and the substrate, which makes it possible to use an inexpensive resin substrate instead of an expensive ceramics substrate.

According to another aspect of the present invention, in order to solve the above-mentioned problem, in a semiconductor device, a semiconductor package is comprised of a substrate for mounting a semiconductor element thereon to fix the semiconductor element to one side thereof, and a connecting pattern provided on the other side of the substrate, the substrate being provided with a through hall formed from the one side to the other side of the substrate, a surface where the element is formed of the semiconductor element being mounted on the one side of the substrate, an electrode of the semiconductor element being fixed to the one side so as to be within the through hall and being electrically connected to the connecting pattern via wires through the through hall, and the through hall and the wires

being sealed with resin.

With this semiconductor device, since the semiconductor package of the present invention described above is used, and the electrode formed on the surface where the element is formed of the semiconductor element and the connecting pattern of the substrate are bonded with wires through the through hall, the wires can be disposed without going around to the outer peripheral side of the semiconductor element. This eliminates the necessity of space for the wires on the outer peripheral side of the semiconductor element.

Further, since the semiconductor element and the substrate are bonded with the wires, the wires can absorb the difference of the coefficient of thermal expansion between the semiconductor element and the substrate, which makes it possible to use an inexpensive resin substrate instead of an expensive ceramics substrate.

According to still another aspect of the present invention, in order to solve the above-mentioned problem, a method of manufacturing a semiconductor device is comprised of the steps of preparing a semiconductor package structured by providing a substrate for mounting a semiconductor element thereon to fix the semiconductor element to one side thereof and

a connecting pattern provided on the other side of the substrate and by forming a through hall from the one side to the other side of the substrate, fixing a surface where the element is formed of the semiconductor element on the one side of the substrate of the semiconductor package such that an electrode of the semiconductor element is within the through hall, electrically connecting the connecting pattern and the electrode of the semiconductor element via wires through the through hall, and sealing the through hall and the wires with resin.

With this method of manufacturing a semiconductor device, since the semiconductor package of the present invention described above is used, and the electrode formed on the surface where the element is formed of the semiconductor element and the connecting pattern of the substrate are bonded with wires through the through hall, the wires can be disposed without going around to the outer peripheral side of the semiconductor element. This eliminates the necessity of space for the wires on the outer peripheral side of the semiconductor element.

Further, since the semiconductor element and the substrate are bonded with the wires, the wires can absorb the difference of the coefficient of thermal expansion between the semiconductor element and the substrate, which makes it possible

to use an inexpensive resin substrate instead of an expensive ceramics substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

Fig. 1 is a sectional side elevation illustrating a schematic structure of a first embodiment of a semiconductor device according to the present invention;

Fig. 2A and B are perspective views of the semiconductor device shown in Fig. 1 for explaining the structure thereof, and particularly, for explaining the rear surface side of a semiconductor package, and Fig. 2C is a perspective view of the semiconductor device shown in Fig. 1 for explaining the structure thereof, and particularly, for explaining the front surface side of the semiconductor package;

Fig. 3 is a perspective view of a semiconductor element illustrating a surface where the element is formed;

Fig. 4 is a perspective view of the semiconductor device for explaining the rear surface side thereof;

Fig. 5 is a perspective view of the semiconductor device for explaining the rear surface side thereof;

Fig. 6 is a sectional side elevation illustrating a schematic structure of a second embodiment of a semiconductor

device according to the present invention;

Fig. 7 is a sectional side elevation illustrating a schematic structure of a third embodiment of a semiconductor device according to the present invention;

Fig. 8 is a sectional side elevation illustrating a schematic structure of an example of a conventional semiconductor device; and

Fig. 9 is a sectional side elevation illustrating a schematic structure of another example of a conventional semiconductor device.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention will now be described in detail.

Fig. 1 illustrates a first embodiment of a semiconductor device according to a fourth aspect of the present invention. In Fig. 1, reference numeral 30 denotes a semiconductor device, and the semiconductor device 30 is formed by mounting a semiconductor element 32 on a semiconductor package 31. It is to be noted that the semiconductor package 31 in the semiconductor device 30 is a first embodiment of a semiconductor package according to the first aspect of the present invention.

In the semiconductor device 30, the semiconductor package

31 comprises a rectangular substrate 33 for mounting the semiconductor element 32 thereon to fix the side of a surface 32a where the element is formed of the semiconductor element 32 to one side thereof, and a plurality of connecting patterns 34 provided on the other side of the substrate 33. The material of the substrate 33 is glass epoxy resin or the like. As shown in Fig. 2A, a through hall 35 is formed along the longitudinal center line of the substrate 33. The through hall 35 is formed as a rectangular opening from the one side to which the semiconductor element 32 is fixed to the other side. It is to be noted that, as shown in Figs. 1 and 2A, the respective connecting patterns 34 are formed so as to extend from longitudinal edge portions of the substrate 33 to the through hall 35, and are made of metal or the like and are conductive.

As shown in Figs. 1 and 2B, an insulating film 36 covering the connecting patterns 34 with the connecting patterns 34 being partly exposed is formed on the other side of the substrate 33 on which the connecting patterns 34 are formed. The insulating film 36 is made of resist or the like, and is provided with end portions 34a of the connecting patterns 34 on the side of the through hall 35 and portions other than the end portions 34a, in this example, end portions 34b opposite to the end

portions 34a, exposed, and with the through hall 35 left opened, i.e., without covering the through hall 35.

As shown in Figs. 1 and 2C, a tape-like bonding material 37 is provided on the one side of the substrate 33 of the semiconductor package 31 thus structured with a portion around the longitudinal center line of the through hall 35 being opened. The bonding material 37 is formed by applying thermoplastic adhesive such as polyamideimide or thermosetting adhesive such as modified epoxy resin on both sides of a tape base material made of resin such as polyimide.

As shown in Fig. 1, the semiconductor element 32 is mounted and fixed via the bonding material 37 on the one side of the substrate 33. As shown in Fig. 3, the semiconductor element 32 is like a rectangular plate with a plurality of electrodes 38 formed on the longitudinal center line of the surface 32a where the element is formed. The electrodes 38 are disposed within the through hall 35.

As shown in Figs. 1 and 4, the electrodes 38 of the semiconductor element 32 disposed within the through hall 35 are connected to the end portions 34a of the connecting patterns 34 via wires 39 through the through hall 35. By this, the electrodes 38 are electrically connected to the connecting

patterns 34.

As shown in Fig. 1, external connecting terminals 40 such as solder balls are connected to the other exposed end portions 34b of the connecting patterns 34. By this structure, the electrodes 38 of the semiconductor element 32 are electrically connected to the external connecting terminals 40 via the wires 39 and the connecting patterns 34.

Further, as shown in Figs. 1 and 5, the through hall 35 through which the wires 39 for connecting the electrodes 38 to the connecting patterns 34 are disposed is filled with insulating resin 41 covering the end portions 34a of the connecting patterns 34. By this, the electrodes 38, the wires 39, and the end portions 34a of the connecting patterns 34 are sealed and insulated from the external.

Next, a method of manufacturing the semiconductor device 30 thus structured is described. It is to be noted that the example of a manufacturing method described herein is an embodiment according to a seventh aspect of the present invention.

First, the semiconductor package 31 shown in Figs. 2A - C and the semiconductor element 32 shown in Fig. 3 are prepared. Here, the tape-like bonding material 37 provided on the one side

of the substrate 33 of the semiconductor package 31 may be provided on the side of the semiconductor element 32 instead of being provided on the side of the substrate 33.

Next, the semiconductor element 32 is mounted on one side of the semiconductor package 31 thus prepared with the electrodes 38 of the semiconductor element 32 being within the through hall 35. Next, by heating and pressurizing them with this state maintained, the substrate 33 of the semiconductor package 31 and the surface 32a where the element is formed of the semiconductor element 32 are made to closely adhere to each other. By melting and solidifying, or by curing, the adhesive of the bonding material 37, the semiconductor element 32 is fixed to the one side of the substrate 33.

Then, as shown in Fig. 4, wire bonding is carried out with respect to the electrodes 38 within the through hall 35 in the substrate 33 and the corresponding end portions 34a of the connecting patterns 34 on the other side of the substrate 33. Next, the electrodes 38 are electrically connected to the connecting patterns 34 via the wires 39 through the through hall 35. It is to be noted that a conventionally used wire bonder may be used to carry out the wire bonding.

Then, as shown in Fig. 5, the through hall 35 is filled

with the insulating resin 41 such as epoxy resin, and the insulating resin 41 is applied so as to cover the wires 38 and the end portions 34a of the connecting patterns 34 to seal all of the electrodes 38, the wires 39, and the end portions 34a of the connecting patterns 34.

After that, the external connecting terminals 40 such as solder balls are bonded to the respective end portions 34b of the connecting patterns 34 under high temperature to obtain the semiconductor device 30.

With the semiconductor device 30 thus obtained, since the electrodes 38 formed on the surface 32a where the element is formed of the semiconductor element 32 and the connecting patterns 34 of the substrate 33 are bonded with the wires 39 through the through hall 35, it is not necessary to provide space for the wires 39 on the outer peripheral side of the semiconductor element 32, which leads to miniaturizing and thinning the device as a whole.

Further, since the semiconductor element 32 and the substrate 33 are bonded with the wires, the wires 39 can absorb the difference of the coefficient of thermal expansion between the semiconductor element 32 and the substrate 33, which makes it possible to use an inexpensive resin substrate instead of an

expensive ceramics substrate.

Fig. 6 illustrates a second embodiment of a semiconductor device according to the fourth aspect of the present invention. The difference between a semiconductor device 50 in Fig. 6 and the semiconductor device 30 shown in Fig. 1 resides in the structure of a semiconductor package 51 in the semiconductor device 50. The semiconductor package 51 in the semiconductor device 50 is a second embodiment of a semiconductor package according to the first aspect of the present invention. The semiconductor package 51 differs from the semiconductor package 31 shown in Fig. 1 in that its connecting patterns 52 are formed in a plurality of stages (two stages in this example).

More specifically, a substrate 53 of the semiconductor package 51 is formed of an upper plate 53a and a lower plate 53b. The lower plate 53b is formed such that its edge on the side of a through hall 54 is outside an edge of the upper plate 53a. By this structure, the rear surface (the other side) of the substrate 53 is formed to be in two stages, i.e., the rear surface of the upper plate 53a and the rear surface of the lower plate 53b.

A first plurality of connecting patterns 52a are provided on the rear surface of the upper plate 53a of the substrate 53.

A second plurality of connecting patterns 52b are provided on the rear surface of the lower plate 53b. The first and the second connecting patterns 52a and 52b are electrically connected to each other via a wiring material 55 provided so as to pierce the lower plate 53b. By this structure, the connecting patterns 52 are in two stages (a plurality of stages) formed by the first connecting patterns 52a, the wiring material 55, and the second connecting patterns 52b.

An insulating film 56 is formed on the rear surface of the lower plate 53b so as to cover the second connecting patterns 52b. It is to be noted that, in this example also, the insulating film 56 is formed with the second connecting patterns 52b being partly exposed, that is, similarly to the one shown in Fig. 2B, with longitudinal end portions of the substrate 53 being exposed.

In the through hall 54 formed with the stages in the substrate 53 formed of the upper plate 53a and the lower plate 53b in this way, the electrodes 38 of the semiconductor element 32 disposed within the through hall 54 are connected via the wires 39 to the end portions of the first connecting patterns 52a exposed on the rear surface of the upper plate 53a of the substrate 53. Further, the through hall 54 is filled with

insulating resin 57 covering the wires 39 and the end portions of the first connecting patterns 52a. By this, the electrodes 38, the wires 39, and the end portions of the first connecting patterns 52a are sealed and insulated from the external.

With the semiconductor device 50 thus structured, similarly to the case of the semiconductor device 30 shown in Fig. 1, since it is not necessary to provide space for the wires 39 on the outer peripheral side of the semiconductor element 32, the device can be miniaturized and thinned as a whole. Further, since the wires 39 can absorb the difference of the coefficient of thermal expansion between the semiconductor element 32 and the substrate 53, an inexpensive resin substrate can be used as the substrate 53.

Still further, since the substrate 53 is formed in two stages of the upper plate 53a and the lower plate 53b, and the connecting patterns 52 are in two stages (a plurality of stages) formed by the first connecting patterns 52a, the wiring material 55, and the second connecting patterns 52b, such that the wires 39 are connected to the end portions to the central side of the substrate 53, that is, to the end portions provided on a stage on the side of the one side of the substrate 53, the wires 39 may be cased within the through hall 54 without extending to the

outside. By this, the wires 39 can be covered with the insulating resin 57 just by filling the through hall 54 with the insulating resin 57 at the bottom of the substrate 53 without heaping up the insulating resin 57 on the rear surface of the lower plate 53b. Accordingly, the diameter of the external connecting terminals 40 such as solder balls can be made small, which leads to finer pitch of the external connecting terminals 40.

Fig. 7 illustrates a third embodiment of a semiconductor device according to the fourth aspect of the present invention. The difference between a semiconductor device 60 in Fig. 7 and the semiconductor device 30 shown in Fig. 1 resides in the structure of a semiconductor package 61 in the semiconductor device 60. The semiconductor package 61 in the semiconductor device 60 is a third embodiment of a semiconductor package according to the first aspect of the present invnetion. The semiconductor package 61 differs from the semiconductor package 31 shown in Fig. 1 mainly in that a plurality of through halls 63, two through halls 63 in this example, are formed in a substrate 62.

More specifically, two lines of the through halls 63 are formed in the substrate 62 of the semiconductor package 61 along

the longitudinal direction of the substrate 62. Connecting patterns 64 are formed and disposed so as to cross the through halls 63 from the outside of the through halls 63 (from the longitudinal sides of the substrate 62) to the central side of the through halls 63. Outside end portions of the connecting patterns 64 are covered with an insulating film 65 with part of them being exposed toward the outside.

Two lines of electrodes 67 are formed on a surface where the element is formed of a semiconductor element 66 mounted on the semiconductor package 61 of the semiconductor device 60. The respective electrodes 67 are disposed within either of the through halls 63 in the substrate 62.

The electrodes 67 are connected to the connecting patterns 64 via the wires 39 through the through halls 63. By this, the electrodes 67 are electrically connected to external connecting terminals 68 connected to the end portions of the connecting patterns 64.

Further, the through halls 63 are filled with insulating resin 69 covering the wires 39 and the end portions of the connecting patterns 64 on the side connected to the wires 39. By this, the electrodes 67, the wires 39, and the end portions of the connecting patterns 64 are sealed and insulated from the

external.

With the semiconductor device 60 thus structured, similarly to the case of the semiconductor device 30 shown in Fig. 1, since it is not necessary to provide space for the wires 39 on the outer peripheral side of the semiconductor element 66, the device can be miniaturized and thinned as a whole. Further, since the wires 39 can absorb the difference of the coefficient of thermal expansion between the semiconductor element 66 and the substrate 62, an inexpensive resin substrate can be used as the substrate 62.

Still further, the semiconductor element 66 in which the electrodes 67 are disposed on the peripheral side instead of the central portion of the semiconductor element 66 as the semiconductor element to be mounted on the semiconductor package 61.

It is to be noted that though the tape-like bonding material 37 is used to fix the semiconductor element on the substrate of the semiconductor package in the embodiments described in the above, the present invention is not limited thereto, and liquid adhesive such as epoxy resin may be used instead of the bonding material 37.

As described in the above, in the semiconductor package

according to s first aspect of the invention, since the through hall is formed in the substrate and the connecting pattern is provided on the side of the substrate opposite to the side on which the surface where the element is formed of the semiconductor element is mounted, an electrode formed on the surface where the element is formed of the semiconductor element and the connecting pattern can be bonded with wires through the through hall. Accordingly, wires can be disposed without going around to the outer peripheral side of the semiconductor element. This eliminates the necessity of securing space for the wires on the outer peripheral side of the semiconductor element, and thus, a semiconductor device using this can be miniaturized and thinned.

Further, since wire bonding can be carried out, the wires can absorb the difference of the coefficient of thermal expansion between the semiconductor element and the substrate, which makes it possible to use an inexpensive resin substrate instead of an expensive ceramics substrate. By this, the cost of the semiconductor device can be lowered.

In the semiconductor device according to the fourth aspect of the invention, since the semiconductor package of the first aspect of the present invention is used, and the electrode

formed on the surface where the element is formed of the semiconductor element and the connecting pattern of the substrate are bonded with wires through the through hall, the wires can be disposed without going around to the outer peripheral side of the semiconductor element. This eliminates the necessity of space for the wires on the outer peripheral side of the semiconductor element, and thus, the device can be miniaturized and thinned as a whole.

Further, since the semiconductor element and the substrate are bonded with the wires, the wires can absorb the difference of the coefficient of thermal expansion between the semiconductor element and the substrate, which makes it possible to use an inexpensive resin substrate instead of an expensive ceramics substrate. By this, the cost of the semiconductor device can be lowered.

In the method of manufacturing a semiconductor device according to the seventh aspect of the invention, since the semiconductor package of the first aspect of the present invention is used, and the electrode formed on the surface where the element is formed of the semiconductor element and the connecting pattern of the substrate are bonded with wires through the through hall, the wires can be disposed without going around

to the outer peripheral side of the semiconductor element. This eliminates the necessity of space for the wires on the outer peripheral side of the semiconductor element, and thus, the device can be miniaturized and thinned as a whole.

Further, since the semiconductor element and the substrate are bonded with the wires, the wires can absorb the difference of the coefficient of thermal expansion between the semiconductor element and the substrate, which makes it possible to use an inexpensive resin substrate instead of an expensive ceramics substrate. By this, the cost of the semiconductor device can be lowered.

What is claimed is:

1. A semiconductor package for fixing a semiconductor element, comprising:

a substrate for mounting said semiconductor element thereon to fix the side of a surface where the element is formed of said semiconductor element to one side thereof, said substrate being provided with a through hall formed from the one side to the other side of the substrate; and

a connecting pattern provided on the other side of said substrate for electrical connection to said semiconductor element.

2. A semiconductor package as claimed in claim 1, wherein said connecting pattern is provided continuously in a plurality of stages and an end portion of said connecting pattern on the side of said through hall is provided on a stage on the side of the one side of said substrate.

3. A semiconductor package as claimed in claim 1, wherein said through hall is a plurality of through halls.

4. A semiconductor device with a semiconductor element fixed to a semiconductor package, said semiconductor package comprising:

a substrate for mounting said semiconductor element

thereon to fix said semiconductor element to one side thereof; and a connecting pattern provided on the other side of said substrate, said substrate being provided with a through hall formed from the one side to the other side of said substrate, wherein a surface where the element is formed of said semiconductor element is mounted on the one side of said substrate, an electrode of said semiconductor element is fixed to the one side so as to be within said through hall and is electrically connected to said connecting pattern via wires through said through hall, and said through hall and said wires are sealed with resin.

5. A semiconductor package as claimed in claim 4, wherein said connecting pattern is provided continuously in a plurality of stages and an end portion of said connecting pattern on the side of said through hall is provided on a stage on the side of the one side of said substrate.

6. A semiconductor package as claimed in claim 4, wherein said through hall is a plurality of through halls.

7. A method of manufacturing a semiconductor device with a semiconductor element fixed to a semiconductor package, comprising the steps of:

preparing said semiconductor package structured by

providing a substrate for mounting said semiconductor element thereon to fix said semiconductor element to one side thereof and a connecting pattern provided on the other side of said substrate and by forming a through hall from the one side to the other side of said substrate;

fixing a surface where the element is formed of said semiconductor element on the one side of said substrate of said semiconductor package such that an electrode of said semiconductor element is within said through hall;

electrically connecting said connecting pattern and said electrode of said semiconductor element via wires through said through hall; and

sealing said through hall and said wires with resin.

8. A method of manufacturing a semiconductor device as claimed in claim 7, wherein said connecting pattern is provided continuously in a plurality of stages and an end portion of said connecting pattern on the side of said through hall is provided on a stage on the side of the one side of said substrate.

9. A method of manufacturing a semiconductor device as claimed in claim 7, wherein said through hall is a plurality of through halls.

10. A method of manufacturing a semiconductor device as

claimed in claim 7, 8, or 9, wherein the surface where the element is formed of said semiconductor element is fixed on the one side of said substrate of said semiconductor package via a tape-like bonding material.

11. A method of manufacturing a semiconductor device as claimed in claim 7, 8, or 9, wherein the surface where the element is formed of said semiconductor element is fixed on the one side of said substrate of said semiconductor package with adhesive.

ABSTRACT OF THE DISCLOSURE

A semiconductor package is comprised of a substrate for mounting and fixing a semiconductor element thereon and a connecting pattern. The substrate is provided with a through hall formed therein. The semiconductor element is fixed with its surface where the element is formed being mounted on the substrate and with its electrode being within the through hall. The electrode of the semiconductor element is electrically connected to the connecting pattern via wires through the through hall. The through hall and the wires are sealed with resin.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION of

Takaaki SASAKI [Group Art Unit: 2822]

Divisional of Serial No. 09/062,720 [Examiner: T. M. Arroyo]

Filed: October 13, 2000

For: SEMICONDUCTOR DEVICE, SEMICONDUCTOR PACKAGE FOR USE THEREIN, AND MANUFACTURING METHOD THEREOF

PROPOSED DRAWINGS REVISIONS

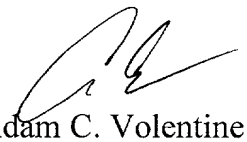
Honorable Assistant Commission of Patents and Trademarks,
Washington, D.C. 20231

Sir:

Kindly amend Figs. 7, 8 and 9 of the drawings of the above-identified application as shown in the marked-up copies of the original Figs. 7, 8 and 9 of the drawings of the above-identified application.

Respectfully submitted,

JONES VOLENTINE, LLC



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Fax No. (703) 715-0877

Date: October 13, 2000

FIG.1

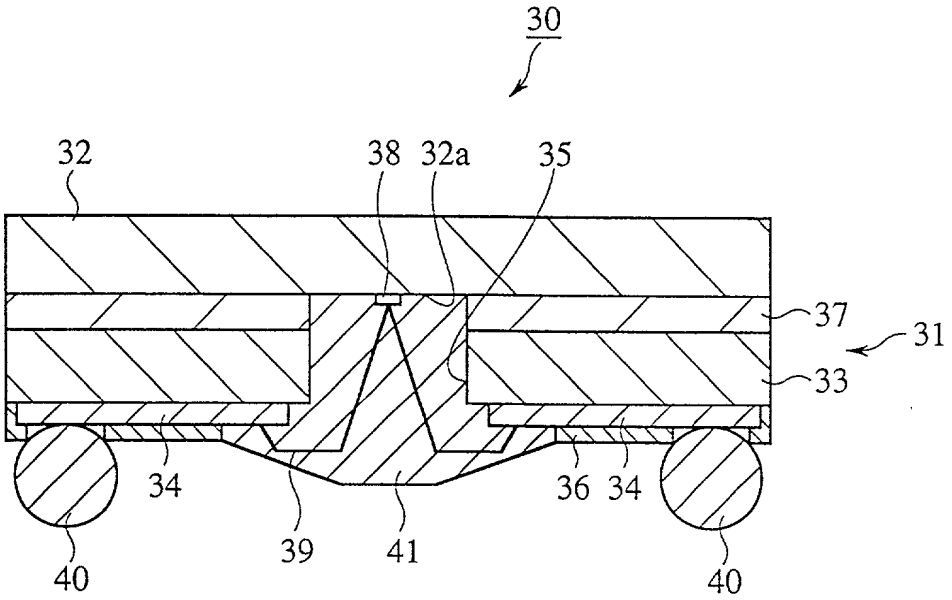

FIG.2A

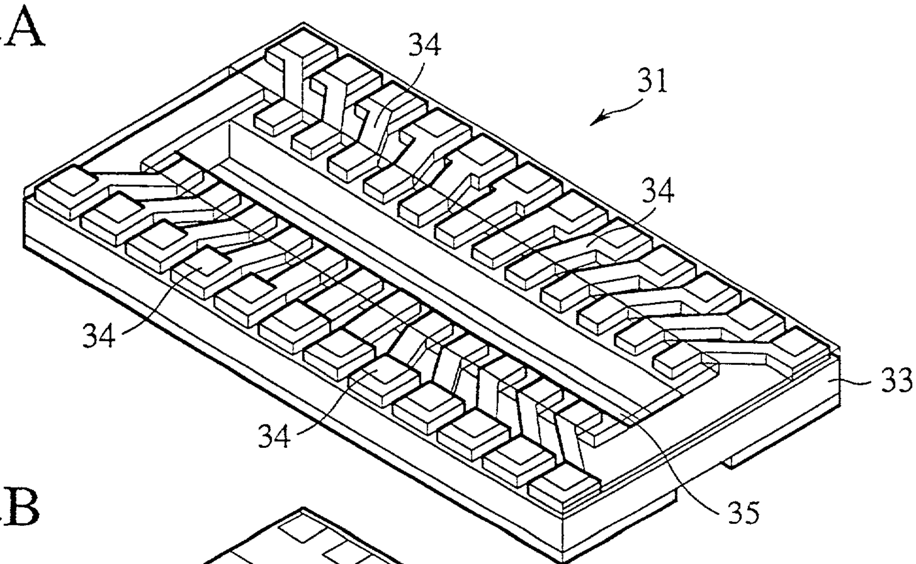

FIG.2B

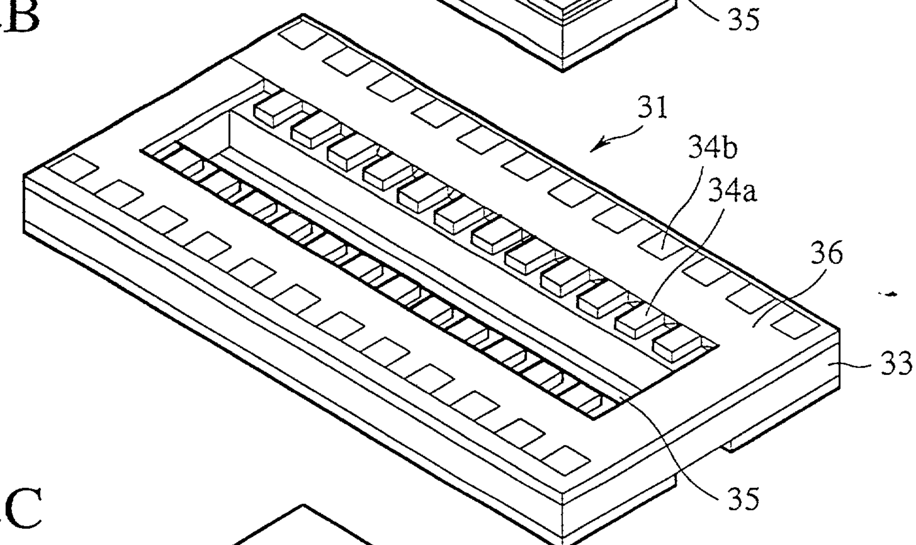

FIG.2C

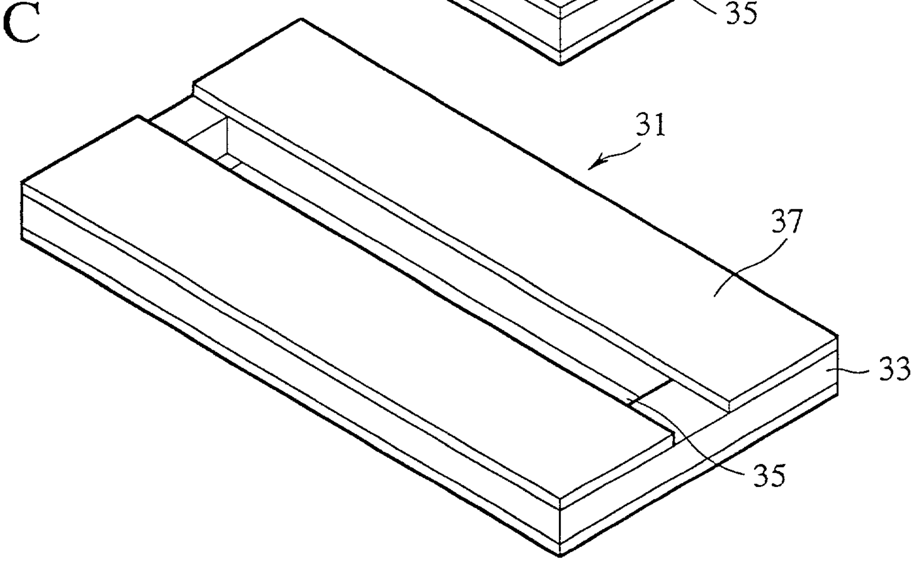

FIG.3

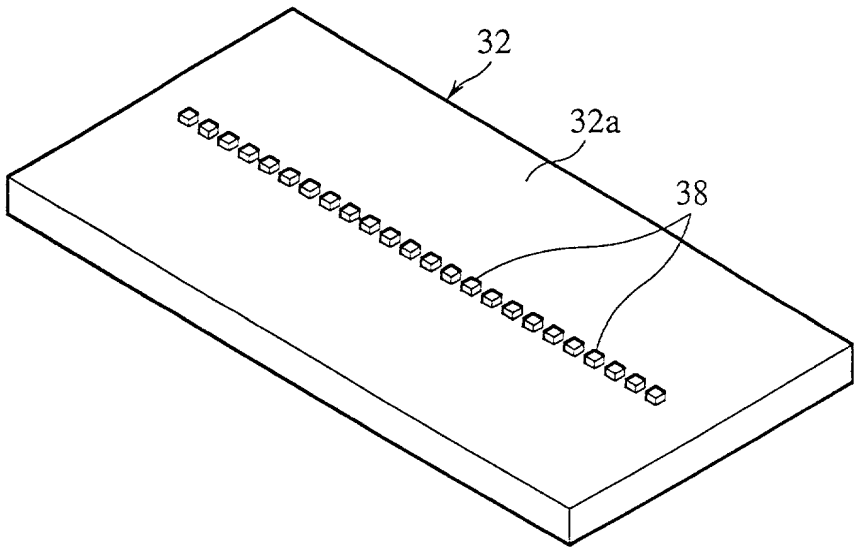

FIG.4

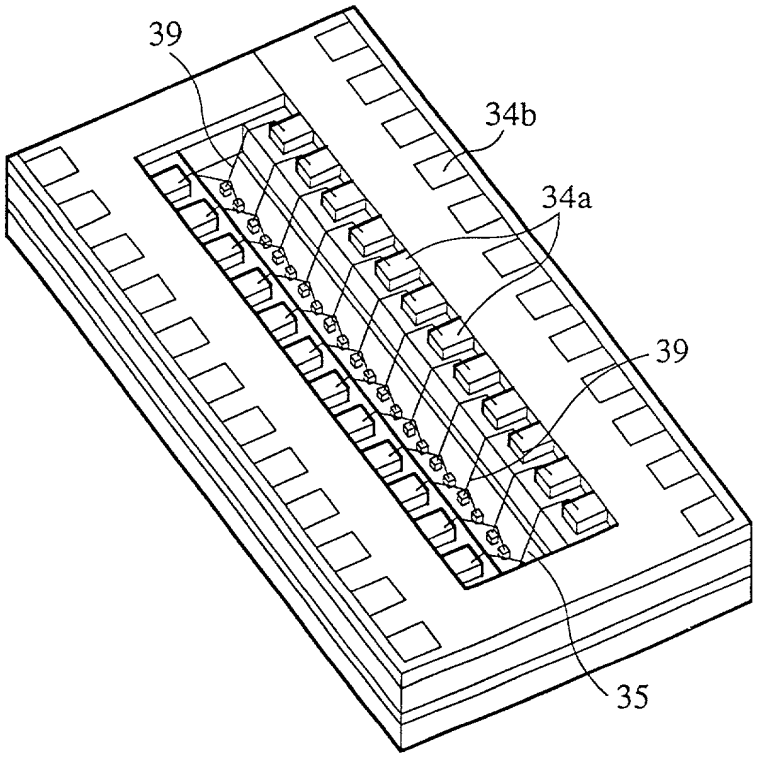

FIG.5

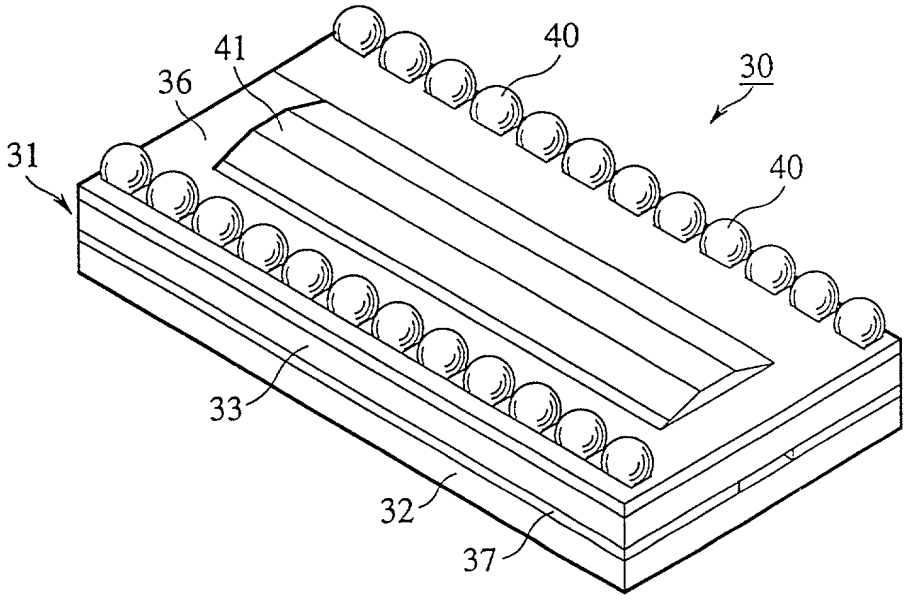
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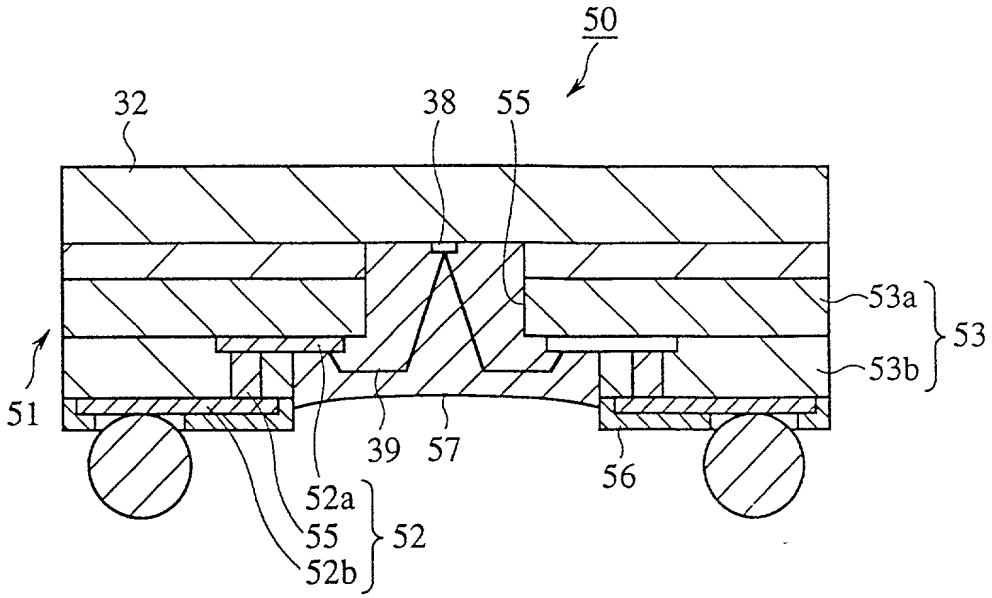
FIG.6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52b

FIG.7

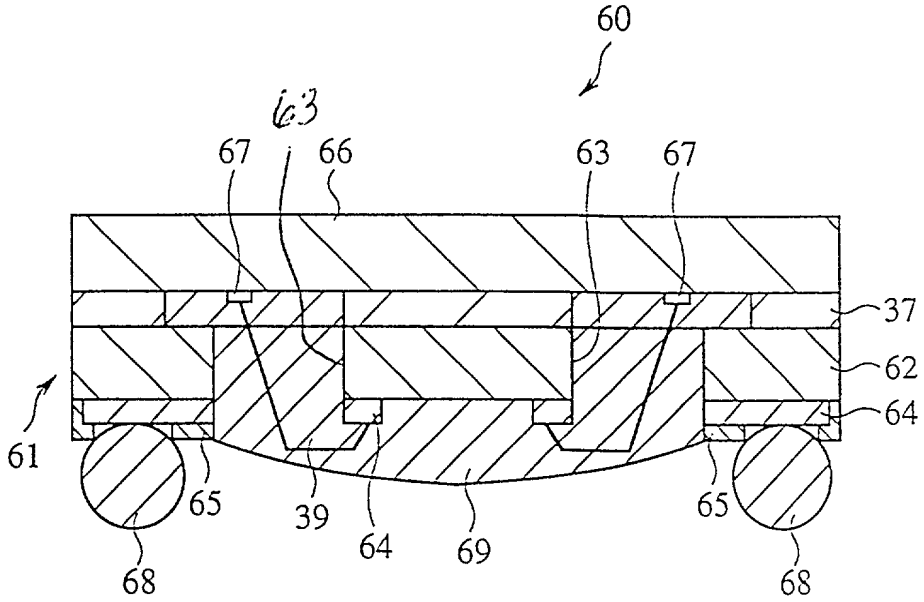
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FIG.8

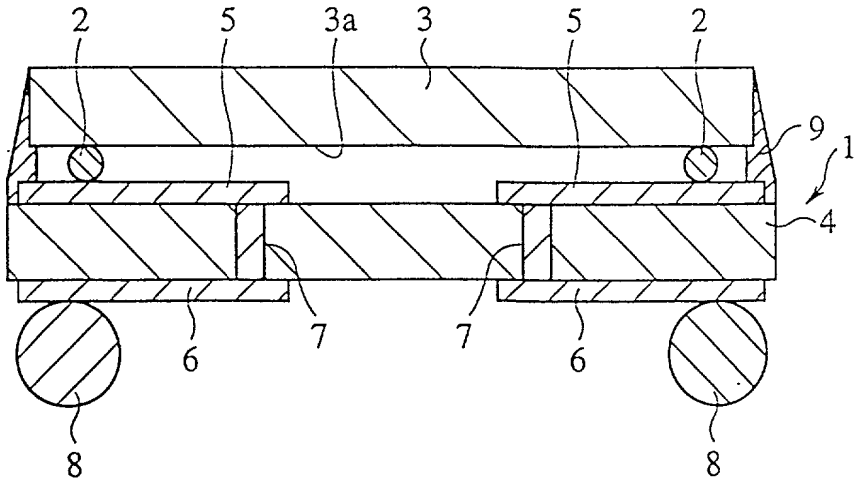
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FIG.9

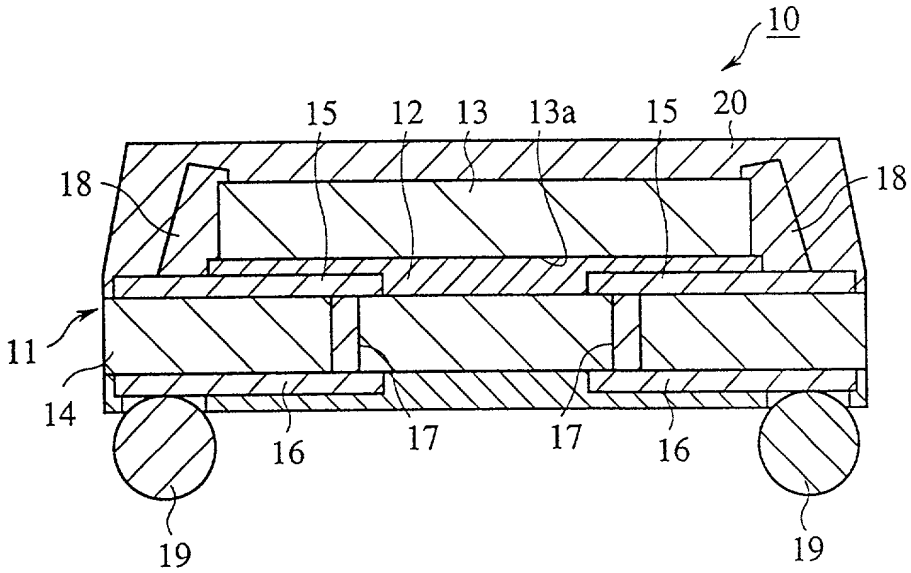

FIG.7

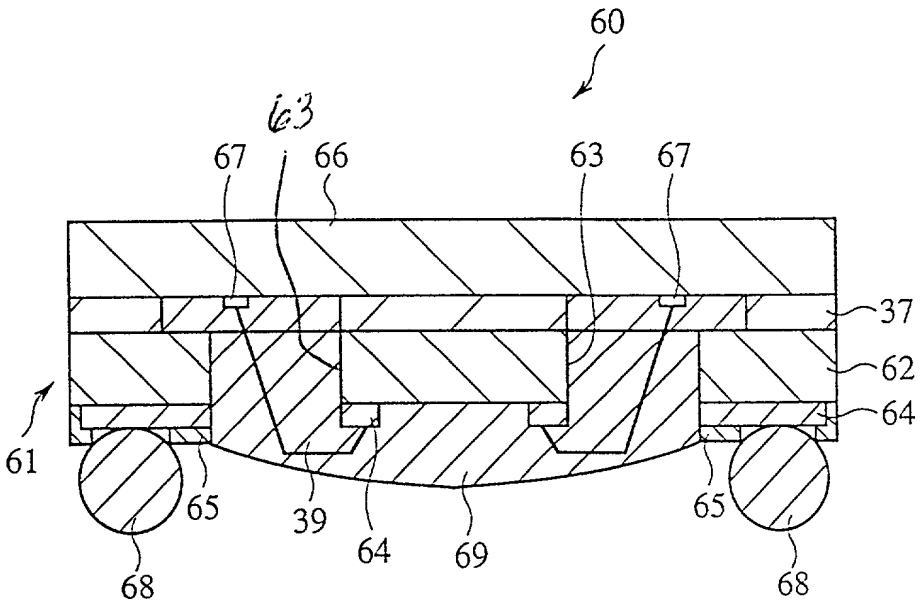
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FIG.8

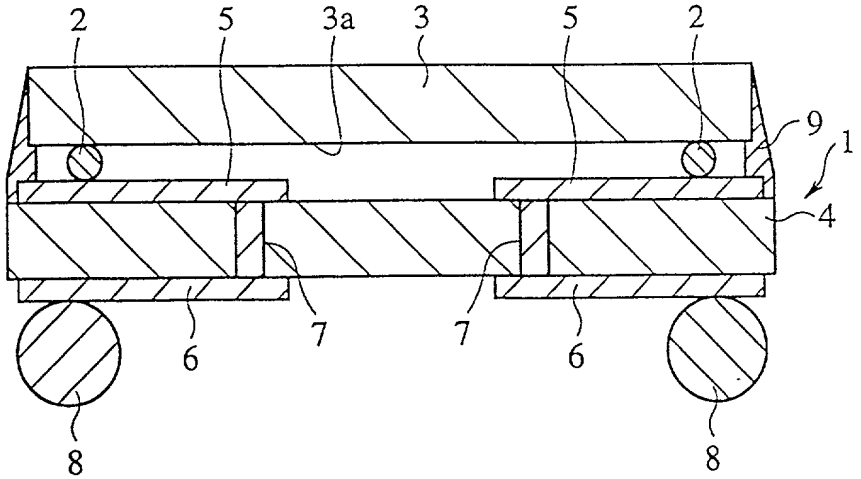
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FIG.7

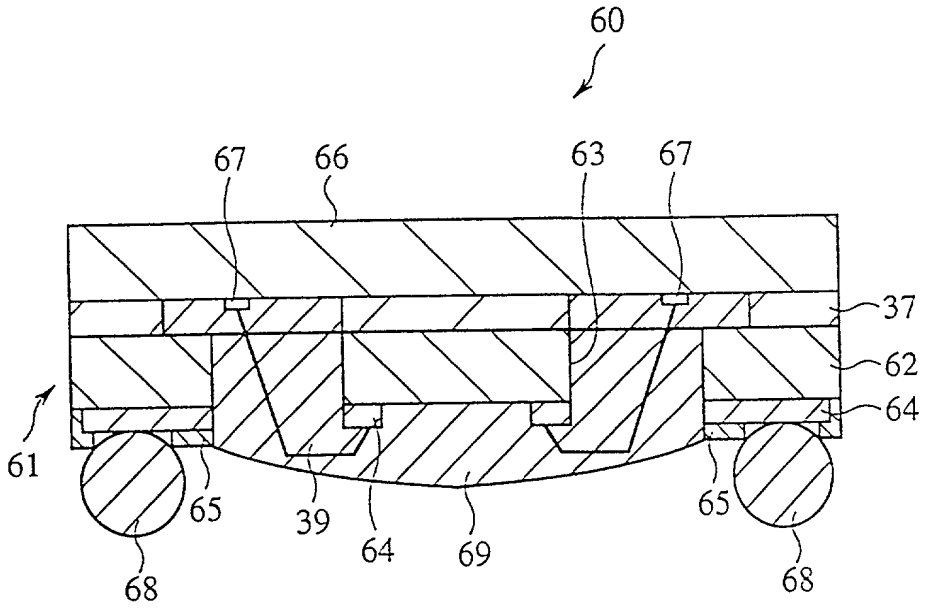


FIG.8 PRIOR ART

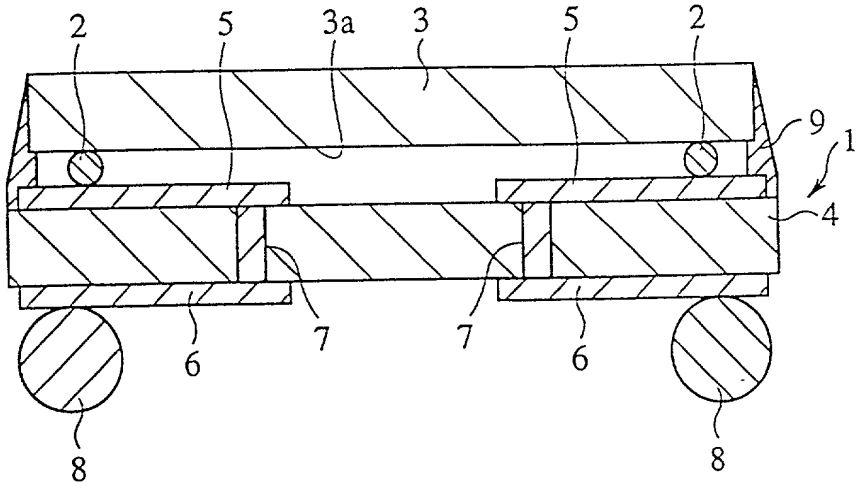
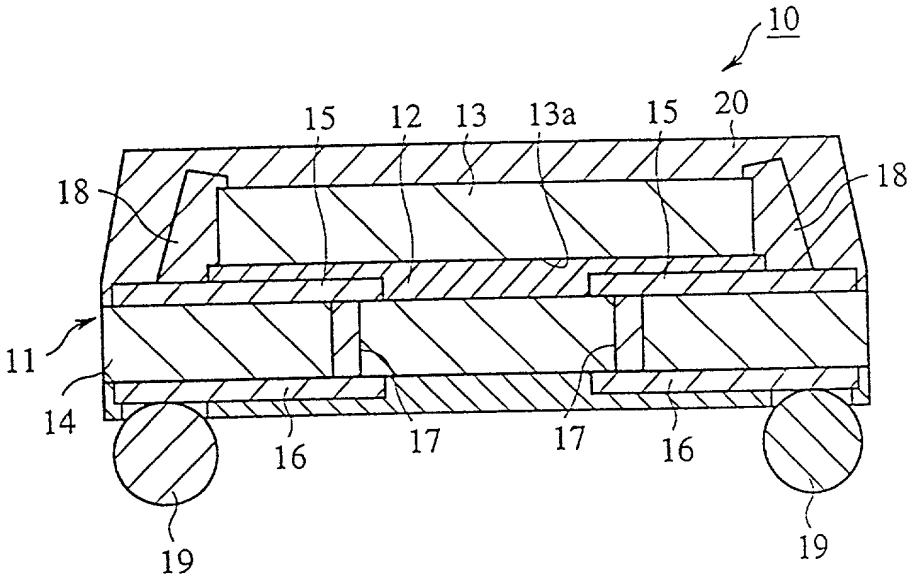


FIG.9 PRIOR ART



DECLARATION AND POWER OF ATTORNEY FOR U.S. PATENT APPLICATION

(X) Original ( ) Supplemental ( ) Substitute ( ) PCT ( ) Design

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

TITLE: SEMICONDUCTOR DEVICE, SEMICONDUCTOR PACKAGE FOR USE THEREIN, AND MANUFACTURING METHOD THEREOF

of which is described and claimed in:

(x) the attached specification, *or*

( ) the specification in the application Serial No._____ filed_____,

and with amendments through_____ (if applicable), *or*

( ) the specification in International Application No. PCT/_____, filed _____,

and as amended on _____ (if applicable).

I hereby state that I have reviewed and understand the content of the above-identified specification, including the claims, as amended by any amendment(s) referred to above.

I acknowledge my duty to disclose information of which I am aware which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 (and §172 if this application is for a Design) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

COUNTRY	APPLICATION NO.	DATE OF FILING	PRIORITY CLAIMED
Japan	H09-190818	July 16, 1997	YES

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION SERIAL NO.	U.S. FILING DATE	STATUS: PATENTED, PENDING, ABANDONED

And I hereby appoint Raymond C. Jones, Reg. No. 34,631 and Adam C. Volentine, Reg. No. 33,289, members of the firm of JONES & VOLENTINE, L.L.P., jointly and severally, attorneys to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected therewith.

I hereby authorize the U.S. attorneys named herein to accept and follow instructions from _____ as to any action to be taken in the U.S. Patent and Trademark Office regarding this application without direct communication between the U.S. attorneys and myself. In the event of a change in the persons from whom instructions may be taken, the U.S. attorneys named herein will be so notified by me.

Kindly direct all correspondence to: **JONES & VOLENTINE, L.L.P.**
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Suite 150
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Telephone (703) 715-0870

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Residence & Citizenship	CITY	STATE OR COUNTRY	COUNTRY OF CITIZENSHIP
Post Office Address	ADDRESS	CITY	STATE OR COUNTRY ZIP CODE
Full Name of 3rd Inventor	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME
Residence & Citizenship	CITY	STATE OR COUNTRY	COUNTRY OF CITIZENSHIP
Post Office Address	ADDRESS	CITY	STATE OR COUNTRY ZIP CODE

Full Name of 4th Inventor	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME	
Residence & Citizenship	CITY	STATE OR COUNTRY	COUNTRY OF CITIZENSHIP	
Post Office Address	ADDRESS	CITY	STATE OR COUNTRY	ZIP CODE

Full Name of 5th Inventor	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME	
Residence & Citizenship	CITY	STATE OR COUNTRY	COUNTRY OF CITIZENSHIP	
Post Office Address	ADDRESS	CITY	STATE OR COUNTRY	ZIP CODE

I further declare that all statements made herein of my own knowledge are true, and that all statements on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

1st Inventor Takaaki Sasaki Date '98.3.19
Takaaki SASAKI

2nd Inventor _____ Date _____

3rd Inventor _____ Date _____

4th Inventor _____ Date _____

5th Inventor _____ Date _____

****

Applicant Reference No.:_____

Atty Docket No.:_____